**PAPER** *Special Section on Analog Circuits and Related SoC Integration Technologies*

# Design of Interpolated Pipeline ADC using Low-Gain Open-Loop Amplifiers

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**SUMMARY** This paper describes the design of an interpolated pipeline analog-to-digital converter (ADC). By introducing the interpolation technique into the conventional pipeline topology, it becomes possible to realize a more than 10-bits resolution and several hundred MS/s ADC using low-gain open-loop amplifiers without any multiplying digital-to-analog converter (MDAC) calibration. In this paper, linearity requirement of the amplifier is analyzed with the relation of reference range and stage resolution first. Noise characteristic is also discussed with amplifier's noise bandwidth and load capacitance. After that, sampling speed and SNR characteristic are examined with various amplifier currents. Next, the resolution optimization of the pipeline stage is discussed based on the power consumption. Through the analysis, reasonable parameters for the amplifier can be defined, such as transconductance, source degeneration resistance and load capacitance. Also, optimized operating speed and stage resolution for interpolated pipelined ADC is shown. The analysis in this paper is valuable to both the design of interpolated pipeline ADCs and other circuits which incorporate interpolation and amplifiers.

***key words:*** *analog-to-digital converter, pipeline topology, interpolation, ADC performance optimization*

## 1. Introduction

8 to 10-bit resolution with a conversion speed of hundreds of mega samples per second ADCs are widely used in wireless communication system. The pipeline ADC topology is suitable for those target specifications. The conventional pipeline ADC requires high gain op-amp for high resolution. For example, more than 70-dB gain from the op-amp is required for a 10-bit resolution pipeline ADC. By technology scaling, digital circuits benefit from high speed, low supply voltage, and small chip area. However, analog circuits suffer from low intrinsic gain and small signal swing due to the short channel effect and the low supply voltage. In the conventional pipeline ADC, insufficient op-amp gain might cause a residue amplification error in a pipeline stage. To realize a high gain op-amp with recent scaled process, several techniques are required such as cascode, gain boosting, and multi stage amplification. Although these techniques are applied, it is difficult to guarantee sufficient gain for high resolution pipeline ADC. Furthermore, wide bandwidth becomes hard to realize with these techniques due to insufficient phase margin.

Recently published pipeline ADCs solve this issue with the addition of calibration circuit. [1] and [2] utilize least mean square (LMS) engine to calibrate capacitor mismatch, insufficient gain of op-amp and op-amp nonlinearity in each MDAC. However, the long time requirement, the large area and the power consumption of the calibration circuit are problematic. For example, [1] needs tens of thousands of clock cycles for calibration. The off-chip calibration circuit consists of approximately 20,000 gates and consumes 8 mW. The work in [2] achieves much less power consumption than [1], such as 1.13 mW. There is no information of the calibration time in [2]; however, it is possible to estimate that similar calibration time in [1] is required because the calibration methods are similar. In [3], the gain coefficients of stages are estimated in foreground calibration before the ADC operation. After the ADC starts its operation, background calibration compensates stage gain errors using coefficients estimated from the foreground calibration. This method reduces calibration time; however, additional MDAC stages are required for calibration and it causes extra power and area.

Several works have reported on calibrating stage gain error in the analog domain. In [4], reference voltage in each pipeline stage is controlled to adjust stage gain. However, this technique is only applicable when the linear settling of the op-amp is guaranteed. Moreover, reference voltage scaling further reduces the voltage swing range of a pipeline stage. Improving op-amp gain by forming positive feedback loop has also been reported in [5]. However, an auxiliary ADC for calibration and complicated calibration circuits degrade its attractiveness. A gain calibration technique of MDAC in [6] tunes feedback capacitance in an op-amp. This calibration requires only 168 clock cycles, which is very small in comparison with the technique in [1]. However, additional capacitance in the output node of the op-amp limits its bandwidth. As explained above, incorporating calibration technique accompanies some disadvantages, such as increasing power consumption, area, complexity, and extra time for calibration.

Recently, two pipeline ADCs, [7] and [8] have reported without MDAC gain calibration. Both of the

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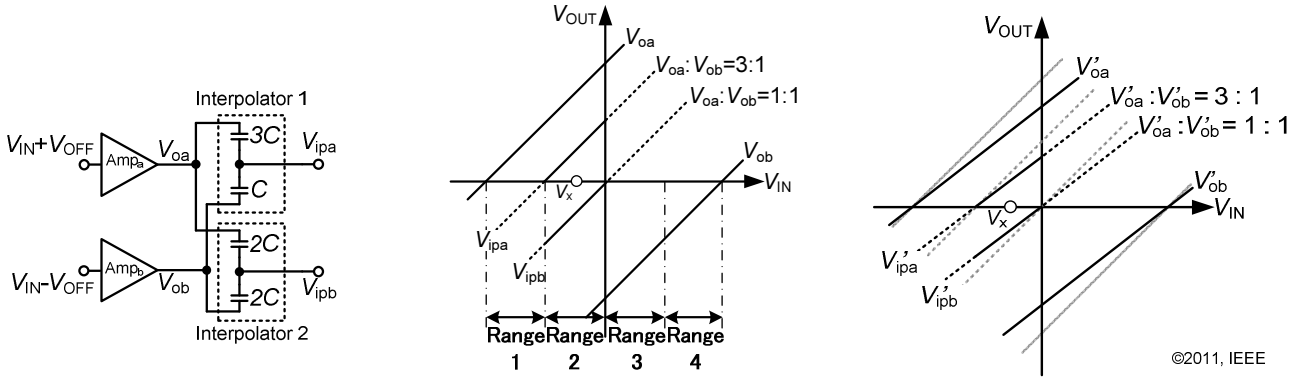



(a) Block diagram of amplifier and interpolator. (b) Example of interpolated signal. (c) Interpolated signals with gain degradation.

**Fig. 1** Circuit and signal examples of interpolation.

ADCs incorporate interpolation technique, which makes it possible to realize more than 10-bit ADCs with relatively low-gain amplifiers. In [7], a 12-bit, 800 MS/s with 4-times interleaved ADC is demonstrated, which is based on [9]-[10]. A 40-dB gain pseudo-differential amplifier is utilized in the MDAC. The offset of the amplifier is calibrated by a 9-bit DAC. In comparison with [7], the pipeline ADC in [8] achieves 10-bit, 320 MS/s using low-gain open-loop amplifiers. A 9.5-dB low-gain amplifier is used in [8] without any calibration. Open-loop topology brings other advantages, such as wide bandwidth and fast response.

In this paper, the design of interpolated pipeline ADC is suggested based on [8]. Section 2 introduces the interpolation technique and the pipeline stage structure. Section 3 analyzes the linearity requirement and the noise characteristic to determine the amplifier's parameters. Section 4 details the effects of the parameter variation of the amplifier to performance of the ADC, such as load capacitance and gain. Section 5 describes the resolution optimization in the pipeline stage. After that, the design flow is suggested in Section 6. Finally, the paper is concluded in Section 7.

## 2. Characteristic of Interpolated Pipeline ADC

### 2.1 Interpolation

Many advantages of the ADC in [8] are based on the interpolation technique. Therefore, it is necessary to figure out a concept of the interpolation for further analysis and discussions.

In circuit design, the interpolation can be defined as to construct a new signal with a certain ratio between two given signals. There are many methods to realize interpolation in circuit design. Fig. 1. (a) shows a circuit example for the 2-bit interpolation in a pipeline stage. Since two sets of signals are necessary for interpolation, there are two amplifiers and two interpolators in the stage. In Fig. 1. (a), the interpolator can be implemented with various components. For example, ADCs in [7], [11]-[15] realize interpolation using resistor ladder. Also, gate-weighted input MOSFETs of comparator is utilized to ADCs in [16]-[17] to realize interpolation. Other interpolation methods have been published in [18]-[20], which incorporate both of resistor ladder and capacitor. In this paper, it is assumed that the interpolator is implemented using capacitor array. The capacitive DAC (CDAC) has advantage of power consumption in comparison with the resistive DAC (RDAC) because there is no static current. Also, the CDAC can work as a sample and hold circuit. Furthermore, the CDAC can be used for the offset cancellation of the amplifier. By those characteristics of the CDAC, the circuit area and the power consumption can be reduced.

Fig. 1. (b) shows an example of interpolated signals from Fig. 1. (a). Assume that signal $V_{IN}$ is inputted to the amplifiers with positive / negative offset voltage, +/- $V_{OFF}$. After that, amplified input signals, $V_{oa}$ and $V_{ob}$ are applied to the interpolators. The interpolators have to output its signal in the proper range based on the voltage level of the input signal. In the pipeline stage, sub-ADC detects the voltage level of the input signal and notifies the interpolator. Then, the interpolator sets the interpolation ratio and the interpolated signal is outputted. The interpolated signal can be define as

$$V_{ipx} = \frac{m(V_{IN}+V_{OFF})+n(V_{IN}-V_{OFF})}{m+n} = \frac{mV_{oa}+nV_{ob}}{m+n} \qquad (1)$$

where $m$ and $n$ are interpolation ratio. $m$ and $n$ can be described as $2^p = m + n$, where $p$ indicates the resolution of the interpolation, such as 2 in Fig. 1. $V_{ipx}$ means $V_{ipa}$ or $V_{ipb}$. For example, the input signal $V_x$ is located in the 2nd reference range within the whole $V_{IN}$ range as shown in Fig. 1. (b), interpolator 1 and 2 divide between $V_{oa}$ and $V_{ob}$ with a ratio of 3:1 and 1:1, respectively. In the conventional pipeline ADC, reference voltages are required to choose reference range. However, in the interpolated pipeline ADC, reference voltage is not necessary as shown in Fig. 1. (b). Following stages repeat the same operations using interpolated signals from the previous stages.

Fig. 1. (c) shows another example of the interpolation with gain degradation of the amplifier. In

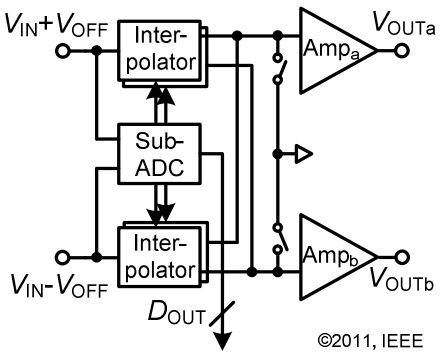



**Fig. 2** Pipeline stage structure.

Fig. 1. (c), the gray colored lines are the original signals and the black colored lines are the gain degraded signals. Even though the gain is changed, the interpolation is completed without any error when two amplifiers' characteristics are matched. This characteristic makes it possible to use low-gain amplifier for the interpolated pipeline ADC with a high resolution target specification.

In this paper, it is assumed that there is no mismatch between two amplifiers. If the amplifiers satisfy the requirements of the linearity, the noise and the settling speed, the matching between two amplifiers are not critical. The gain mismatching might affect to the performance of the ADC; however, the gain matching issue is out of the main topic in this paper.

### 2.2 Interpolated Pipeline Stage

Fig. 2 shows the structure of a pipeline stage in the interpolated pipeline ADC, which utilizes open-loop amplifiers. The pipeline stage consists of amplifiers, sub-ADC, and interpolators. As explained in Fig. 1. (a), two amplifiers and interpolators are incorporated for interpolation. Only single-ended voltages are described in Fig. 2.

Since the interpolation technique does not require reference voltage, the sub-ADC cannot use the conventional comparison method which is comparing input with reference voltage. In [7], dual-residue amplifier outputs are connected to a resistor ladder, and comparator uses the divided voltages in the ladder for its comparison. In contrast, the ADC in [8] utilize capacitor array for interpolation. Therefore, it is difficult to make such kind of reference voltages. A comparator with gate-weighted interpolation technique in [16-17] is incorporated in [8].

#### 2.2.1 CDAC in Interpolated Pipeline Stage

Fig. 3 shows the structure of the CDAC, which is incorporated to the pipeline stage in [8]. A weight controlled topology is used to reduce the total capacitance. The total number of unit capacitors is $2^{N1st}$, where $N_{1st}$ means the resolution of the stage. For 3-bit interpolation, 8 unit capacitors are necessary in each

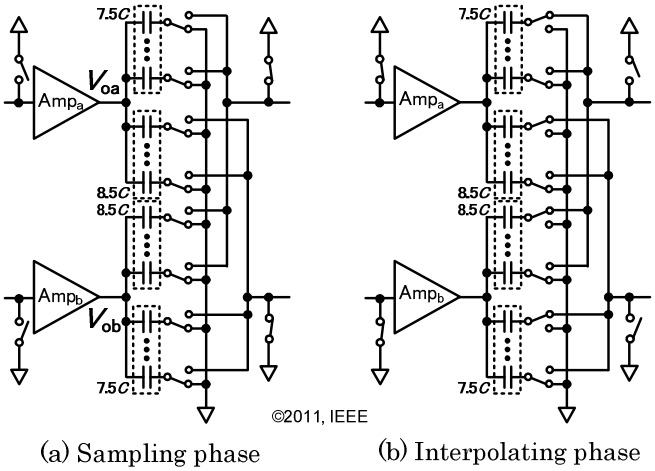
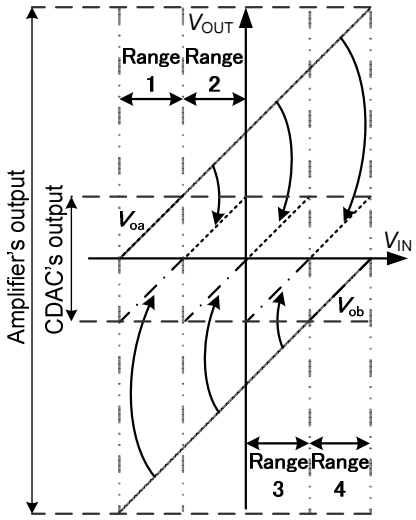



**Fig. 3** Structure and operation of CDAC (3-bit).

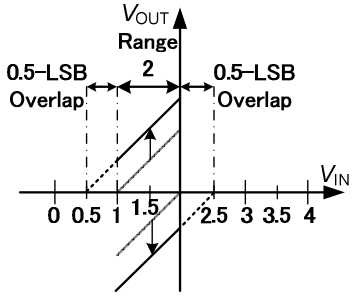
CDAC. In Fig. 3, the total capacitance in each CDAC has +/- 0.5 *C* differences. This is due to the redundancy structure which is explained below. The switches connected to the unit capacitors are reference selection switches. The CDAC has two operation phases, sampling phase and interpolating phase. During the sampling phase, the output signal of the amplifier is charged into all of the unit capacitors. After that, during the interpolating phase, the CDAC generates interpolated signal. The interpolation ratio is controlled by the results of the sub-ADC in the stage. The output signal of the CDAC is represented in (1).

One of the characteristics of the CDAC is shifting the output voltage to the middle of the output signal swing range. This characteristic is shown in Fig. 4. (a). The shifted signals are much more linear due to the linearity characteristic of the amplifier. The linearity of the amplifier is inversely proportional to the output swing range. Another characteristic of the CDAC in the interpolated pipeline topology is one least significant bit (LSB) redundancy structure. In Fig. 4. (a), if there is an offset in the comparator, the CDAC's output signal goes out of its proper range. To solve this issue, one LSB redundancy structure is introduced to the CDAC.

The offset voltage for redundancy is generated by additional weight control. To realize redundancy, each CDAC has a difference of 0.5 *C*. During the interpolating phase, these capacitance differences generate 0.5-LSB shifting. This operation can be expressed in (1) by adding an amount of 0.5-LSB voltage in the numerator. Fig. 4. (b) shows the operation of the redundancy structure using the signals in the range 2. The interpolated signals are shifted by (positive / negative) 0.5-LSB resolution of the stage. This relaxes the offset requirement for the comparator in the sub-ADC. To realize the redundancy, the number of capacitors for one extra bit are required. For example, the number of capacitors for a 3-bit CDAC are necessary to realize a 2-bit CDAC with 1-LSB redundancy.




(a) Voltage shifting to middle of output range.




(b) One LSB redundancy.

**Fig. 4** Characteristics of CDAC.

2.3 ADC Performance

In Section 2, characteristics and advantages of the interpolated pipeline ADC is reviewed. Although A/D conversion in the pipeline stage is not affected by the gain of the amplifier, other characteristics of the amplifier are still crucial for the performance of the ADC, such as the linearity and the noise. In the following analysis, the effects of the amplifier's characteristics to the ADC's performance are examined.

Before starting the analysis, it is useful to define the general definition of the ADC performance. The total noise of the ADC including the quantization noise and the amplifier's error, $v_{n\_total}$ is

$$\boldsymbol{v}_{n\_total}^2 = \frac{\boldsymbol{v}_q^2}{12} + \boldsymbol{v}_{err}^2 \qquad (2)$$

where $v_q$ is the LSB of the ADC and $v_{err}$ is the sum of the amplifier's errors, such as the distortion, the noise, and the offset. In (2), by substituting $\alpha v_q$ for $v_{err}$, the formula can be expressed as a function of $v_q$. $\alpha$ is a coefficient of the amplifier's error. By using the total noise power in (2) and power of sine wave, the SNR definition of the ADC will be

$$\mathrm{SNR} = 10\log_{10}\left(\frac{2^{2N}}{\frac{2}{3}+8\alpha^2}\right) \qquad (3)$$

where $N$ is the resolution of the ADC. Equation (3) indicates that SNR of the ADC degrades by increasing the amplifier's error. Effective number of bit (ENOB) definition can be derived from (3) as below,

$$\mathrm{ENOB} = \boldsymbol{N} - \frac{1}{2}\log_2\left(1+12\alpha^2\right). \qquad (4)$$

More detailed effect of the amplifier's error will be analyzed in the following section with circuit models and formulas. Some characteristics of the ADC are assumed as below for further analysis. In the pipeline stage, the following analysis use the 1st stage, which is the most crucial in the ADC performance. Analysis is also applicable for the following stages because those stages also have the same structure. It is assumed that the CDAC has a reasonably small mismatch to achieve the target specification. The assumption is reasonable because the mismatch of the CDAC can be calibrated easily by digital circuit, unlike nonlinearity. Also, assume that the offset of the comparator is about 1.5 mV ($\sigma$). The offset of the amplifier is assumed to be cancelled by the offset cancelation technique, such as output offset cancellation. Simulations are performed using transistor model. However, for the ADC simulation in Section 4.1, the digital logics are changed to the ideal model to reduce the simulation time. The power consumption of the dynamic type comparator in Section 5 is estimated in [8] at 320 MS/s operating speed. Also, all parameters listed in the table 1 are estimated from the circuits in [8].

## 3. Amplifier

3.1 Topology

Even though the interpolation technique solves the gain issue, if the input signal of the interpolator includes distortion, the ADC performance degrades. There are several reasons to cause the distortion of the amplifier. In the interpolated pipeline ADC, the most severe characteristic is the linearity because low-gain open-loop amplifiers are used.

Several works have been published for the linearity improvement of the amplifier. The multiple input floating gate (MIFG) transistors [21] are used for a large input swing range; however, this technique requires additional process. A double pseudo differential pair CMOS operational transconductance amplifier (OTA) also is introduced in [22]. The pseudo differential pair OTA realizes good linearity using simple structure. However, the balance of the differential pair can collapse easily due to the mismatch of the transistors. Considering the use of the standard CMOS process and robustness, one good choice is source degeneration technique. In this

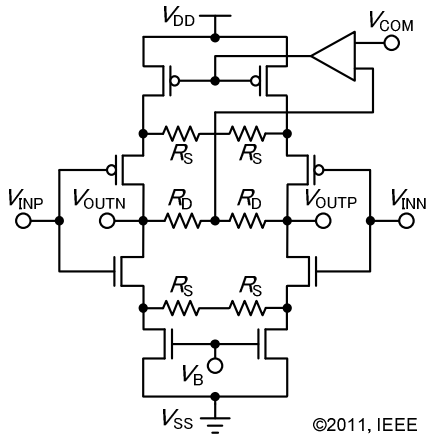



**Fig. 5** Schematic of amplifier.

section, the amplifier with source degeneration is analyzed with interpolated pipeline scheme.

Fig. 5 shows the schematic of the amplifier, which is used in [8]. The amplifier incorporates single stage differential structure without feedback loop. Since it uses single stage topology, it is unnecessary to care about phase margin. The gain of the amplifier is only 9.5-dB. The simple structure in Fig. 5 represents one of the advantages of the interpolated pipeline ADC.

In Fig. 5, $V_B$ is the bias voltage for the current source, $R_S$ is the source degeneration resistance, and $R_D$ is the output resistance. The amplifier has CMOS input to increase $g_m$. The effective $g_m$ ($g_{m\_eff}$), DC-gain ($G_0$), and 3-dB bandwidth ($\omega_{p1}$) are given by

$$g_{m\_eff} = \frac{1}{R_s}\frac{1}{1+\frac{1}{g_m R_s}} \tag{5}$$

$$G_0 = \frac{R_D}{R_S}\frac{1}{1+\frac{1}{g_m R_S}} \tag{6}$$

$$\omega_{p1} = \frac{1}{R_D C_L} \tag{7}$$

where $C_L$ is the load capacitance of the amplifier. It is well known that for the source degeneration amplifier, if the $g_m R_S$ is large enough, the $g_{m\_eff}$ is determined by $R_S$. Also, the gain is determined by the ratio of $R_S$ and $R_D$. The 3-dB bandwidth is determined by $R_D$ and $C_L$.

In the following analysis, the amplifier's gain is set to 3 which is the same value in [8]. In [8], the 3-times gain is enough to achieve less than 1/4 LSB input referred comparator's offset, even though the signal degradation by the input parasitic capacitance of the amplifier is considered. The offset voltage of the comparator is caused by the comparator's mismatch and the calibration circuit. If the offset is varied, the gain of the amplifier should be reconsidered. At that time, the values of $R_S$ and $R_D$ have to be assigned by proper calculation. The effect of $R_D$ will be discussed in detail in Section 4.2.

### 3.2 Linearity

To examine the linearity of the amplifier, it is necessary to define the distortion of the amplifier first. The output voltage of the amplifier including nonlinearity can be defined as below,

$$V_{out} = a_1 V_{in} - a_3 V_{in}^3. \tag{8}$$

In (8), the 1st order and the 3rd order terms are considered because they are dominant. The 2nd order term is omitted by the differential structure of the amplifier. The amount of the distortion caused by the amplifier's 3rd harmonic can be represented by $a_3/a_1$. $a_3/a_1$ can be calculated using the current formula of the MOS transistor. The current in the differential amplifier without source degeneration, $\Delta I_{out}$ is

$$\Delta I_{out} = \frac{K}{2}\Delta V_{in}\sqrt{\frac{4I_s}{K} - \Delta V_{in}^2} \tag{9}$$

where

$$K = \mu C_{ox}\frac{W}{L}. \tag{10}$$

In (9), $I_S$ is the sink current. The output voltage of the amplifier, $\Delta V_{out}$ using Taylor series until 3rd order, can be written as

$$\Delta V_{out} = R_D \Delta I_{out} \approx \sqrt{KI_s}\,R_D \Delta V_{in} - \frac{1}{8}\sqrt{\frac{K^3}{I_s}}R_D \Delta V_{in}^3. \tag{11}$$

In (11), $a_1$ and $a_3$ are written as below.

$$a_1 = \sqrt{KI_s}\,R_D. \tag{12}$$

$$a_3 = \frac{1}{8}\sqrt{\frac{K^3}{I_s}}R_D. \tag{13}$$

Based on (12) and (13), $a_3/a_1$ can be represented as

$$\frac{a_3}{a_1} = \frac{1}{8(V_{gs}-V_{th})^2}. \tag{14}$$

Equation (14) represents the $a_3/a_1$ without the source degeneration resistance. By introducing the source degeneration resistor, a negative feedback path is formed between the gate and the source node in the input MOS transistor. Therefore, the amount of distortion is reduced by the feedback loop gain; it means $a_3/a_1$ is reduced by $(1+g_m R_S)$. $a_3/a_1$ for the source degeneration topology can be rewritten as

$$\frac{a_3}{a_1} = \left(\frac{1}{1+g_m R_s}\right)\frac{1}{8(V_{gs}-V_{th})^2}. \tag{15}$$

If the amplifier does not incorporates source degeneration, $R_S$ in (15) becomes 0, then (15) becomes equal to (14). At that time, the $a_3/a_1$ is determined by $V_{gs}$ and $V_{th}$. This means the distortion varies with input signal level, and it degrades the linearity characteristic. However, by introducing the source degeneration resistor, the distortion is divided by $(1+g_m R_S)$. Therefore, the source degeneration amplifier can achieve better linearity characteristic.

The calculation and the simulation results of

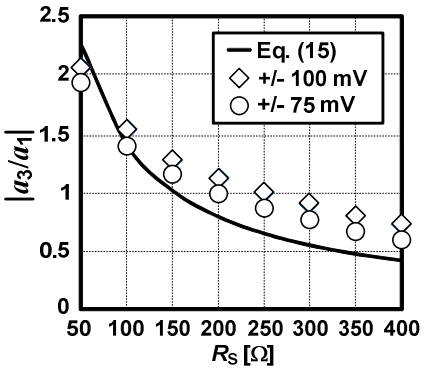



**Fig. 6** $R_S$ vs. distortion of amplifier.

(15) are shown in Fig. 6. The simulation is performed in two input signal range conditions, +/- 75 mV and +/- 100 mV. In the simulation, $R_D$ is assigned 400 Ω which is the same value in [8]. As analyzed in (14)-(15), the linearity characteristic becomes better with increasing $R_S$. The wide signal range degrades linearity characteristic. Therefore, large $R_S$ and small signal range is preferred for better linearity characteristic. There is a small difference between the calculation and the simulation. These differences are caused by $g_m$, which is fixed in the calculation, but it varies in the simulation. The largest difference is 0.2 in +/- 75 mV input signal range which is the same condition in [8]. This means the analysis is usable.

Equation (15) can be rewritten in (16) using the relation of ($V_{gs}$-$V_{th}$) and current,

$$\frac{a_3}{a_1}=\left(\frac{1}{1+g_m R_s}\right)\left(\frac{g_m^2}{32 I_D^2}\right). \tag{16}$$

Equation (16) shows that it is difficult to achieve good linearity characteristic with small current. Therefore, large power consumption is essential for good linearity.

Next, the relationship between the amplifier's linearity and the ADC's performance is analyzed. To investigate the effect of the amplifier's linearity to the performance of the interpolated pipeline ADC, the characteristic of the interpolation has to be considered. Unlike the conventional pipeline ADC, the interpolated pipeline ADC uses two sets of differential signal. The input referred distortion of the amplifier; $\Delta V_{IN}$ can be written by considering 3rd order distortion as shown in (8),

$$\Delta V_{IN}=\frac{m}{m+n}\frac{a_3}{a_1}\left(V_{IN}-V_{OFF}\right)^3+\frac{n}{m+n}\frac{a_3}{a_1}\left(V_{IN}+V_{OFF}\right)^3. \tag{17}$$

In (17), $m$ and $n$ are the ratio of the interpolation and $V_{OFF}$ is the offset voltage for the interpolation. The $V_{OFF}$ is used as the same concept in Fig. 1. Equation (17) can be rearranged to the following,

$$\Delta V_{IN}=8m(M-m)(2m-M)\frac{a_3}{a_1}\left(\frac{V_{OFF}}{M}\right)^3 \tag{18}$$

where

$$M=m+n,\ V_{IN}\approx\frac{2m-M}{M}V_{OFF},\ V_{OFF}=\frac{V_{FS}}{2^{N_{1st}}}. \tag{19}$$

In (19), $V_{FS}$ is the full-scale reference range and $N_{1st}$ is the resolution of the 1st stage. The input referred distortion of the amplifier is proportional to the amplifier's linearity coefficient, $a_3/a_1$. Furthermore, the terms of signal swing range, $V_{OFF}$ and $M$ are more crucial, since they are cubed. Therefore, to achieve better linearity characteristic, small $a_3/a_1$ of the amplifier and increasing the resolution of the stage are effective.

The averaged input referred distortion by using (18) is equal to

$$\overline{\Delta V_{IN}}=\frac{2}{M}\int_{M/4}^{3M/4}\Delta V_{IN}\,dm=0. \tag{20}$$

In (20), the integration range, 3$M$/4 to $M$/4 is determined by the result of considering a 1-LSB redundancy. The averaged noise power is

$$\overline{v_n^2}=\frac{2}{M}\int_{M/4}^{3M/4}\left(\Delta V_{IN}-\overline{\Delta V_{IN}}\right)^2 dm=\frac{407}{1680}\left(\frac{a_3}{a_1}V_{OFF}^3\right)^2. \tag{21}$$

To calculate the effect of the noise power from the amplifier's distortion on the ADC's performance, the formula of the ENOB in (4) can be used. Before using (4), the averaged noise power is necessary to be normalized to $v_q$. After that, the normalized averaged noise power is substitute for α in (4). Then, (4) can be rearranged as

$$\mathrm{ENOB}\approx N-\frac{1}{2}\log_2\left\{1+2.9\left(\frac{a_3}{a_1}V_{FS}^2 2^{N-3N_{1st}}\right)^2\right\}. \tag{22}$$

The calculation and the simulation results of the ENOB vs. the linearity of the amplifier are shown in Fig. 7. The calculation and the simulation are performed in 10-bit resolution. In Fig. 7, about 2.5 of $a_3/a_1$ is enough to achieve 0.2-bit ENOB degradation when $V_{FS}$=0.8 V. The requirement of $a_3/a_1$ becomes more relaxed to 4 when $V_{FS}$ becomes 0.6 V.

By (22) and Fig. 7, the relationship of amplifier's linearity, reference range, and resolution of the stage is analyzed. To achieve better ENOB, reducing $a_3/a_1$ and reference range are effective, because the bad 3rd harmonic and the large reference range degrade the amplifier's linearity characteristic. The high resolution of stage is also effective for better performance. This is because the output signal range of the CDAC is reduced by $2^{N1st}$ as shown in Fig. 4. (a). However, reference range is usually determined by system specification and increasing stage resolution affects other parameters, such as smaller offset requirement for the comparators, increasing power consumption and complexity.

### 3.3 Noise

The noise of the amplifier is another important characteristic to achieve high ENOB of the ADC.

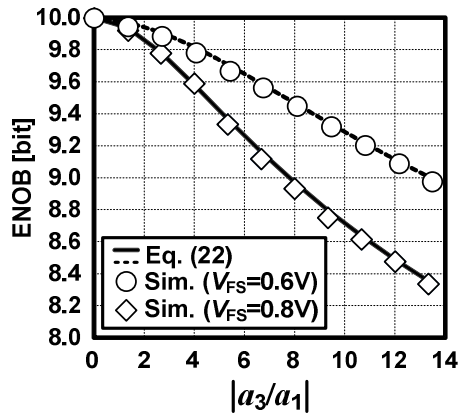



**Fig. 7** ENOB vs. linearity of amplifier.

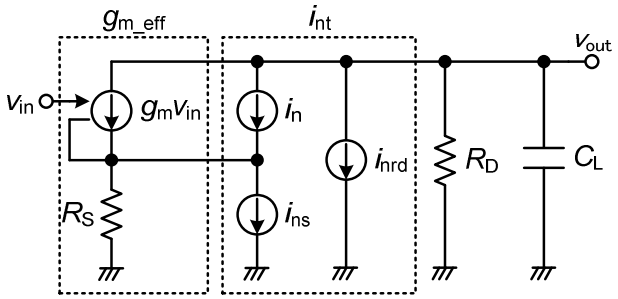



**Fig. 8** Noise analysis model for source-degeneration amplifier.

Especially, since the amplifier topology in the interpolated pipeline ADC is different to the conventional pipeline ADC, the noise characteristic has to be calculated by the structure used in the ADC.

To analyze the noise characteristic of the amplifier, a noise model is necessary. Fig. 8 shows the noise analysis model of the amplifier which is introduced in Fig. 5. In Fig. 8, $g_m$ is the transconductance of the input MOS transistor, $i_n$ is the noise current in the input MOS transistor, $i_{ns}$ is the noise current of the current source and $R_S$, and $i_{nrd}$ is the noise current of $R_D$. The input referred noise spectrum density with regard to $i_n$, $i_{ns}$, and $i_{nrd}$ are expressed as below.

$$\overline{\boldsymbol{v}_{ni}^{\,2}} = \left(\frac{\overline{\boldsymbol{i}_n}}{g_m}\right)^2. \tag{23}$$

$$\overline{\boldsymbol{v}_{nsi}^{\,2}} = \left(\frac{\boldsymbol{v}_{nso}}{\boldsymbol{G}_0}\right)^2 = \boldsymbol{R}_S^{\,2}\overline{\boldsymbol{i}_{ns}^{\,2}}. \tag{24}$$

$$\overline{\boldsymbol{v}_{nrdi}^{\,2}} = \overline{\boldsymbol{i}_{nrd}^{\,2}}\left(\boldsymbol{R}_s + \frac{1}{\boldsymbol{g}_m}\right)^2. \tag{25}$$

The total input referred noise power with consideration of the bandwidth will become

$$\boldsymbol{v}_{nit}^{\,2} = \left(\overline{\boldsymbol{v}_{ni}^{\,2}} + \overline{\boldsymbol{v}_{nsi}^{\,2}} + \overline{\boldsymbol{v}_{nrdi}^{\,2}}\right)\Delta\boldsymbol{f} \tag{26}$$

where

$$\Delta\boldsymbol{f} = \frac{1}{4\boldsymbol{R}_D\boldsymbol{C}_L}. \tag{27}$$

Through (23) to (25), it is recognized that each noise spectrum density is affected by $g_m$ and $R_S$. Detailed discussion to determine $g_m$ and $R_S$ is described in Section 6.

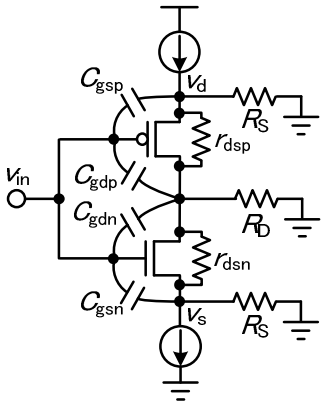



**Fig. 9** Small signal model for input parasitic capacitance analysis.

### 3.4 Input Parasitic Capacitance

The linearity improvement by the source degeneration is explained in Section 3.2. It also reduces the input parasitic capacitance of the amplifier. A small signal model of the amplifier in Fig. 5 with consideration of the parasitic capacitance is presented in Fig. 9.

By adding the source degeneration resistor, the Miller effect occurs to both gate-drain capacitance and gate-source capacitance. For accurate analysis, drain resistance of the MOS transistor is also considered. The gain of gate-drain ($G_d$) and gate-source ($G_s$) can be represented in (28) and (29), respectively.

$$\boldsymbol{G}_d = -\frac{\boldsymbol{g}_m\boldsymbol{R}_D}{1+(\boldsymbol{g}_m+\boldsymbol{g}_{ds})\boldsymbol{R}_S+\boldsymbol{g}_{ds}\boldsymbol{R}_D}. \tag{28}$$

$$\boldsymbol{G}_s = \frac{\boldsymbol{g}_m\boldsymbol{R}_S}{1+(\boldsymbol{g}_m+\boldsymbol{g}_{ds})\boldsymbol{R}_S}\left(1+\frac{\boldsymbol{g}_{ds}}{\boldsymbol{g}_m}\boldsymbol{G}_d\right). \tag{29}$$

$$\boldsymbol{C}_{pi\_total} = (1-\boldsymbol{G}_d)\boldsymbol{C}_{gd} + (1-\boldsymbol{G}_s)\boldsymbol{C}_{gs}. \tag{30}$$

Through (28) and (29), $1/r_{dsp}$ and $1/r_{dsn}$ are assumed the same value, and it is represented as $g_{ds}$. In (30), $C_{pi\_total}$ means the total input parasitic capacitance. $C_{pi\_total}$ can be calculated by adding up $C_{gs}$ and $C_{gd}$ with consideration of the Miller effect. The calculation and the simulation results are shown in Fig. 10. In Fig. 10, the total input parasitic capacitance is reduced with increasing $R_S$. For example, when $R_S$ varies from 0 to 200 Ω, the total input capacitance is reduced from 113 fF to 36 fF.

The input parasitic capacitance reduces the input signal swing range and the SNR. When the amplifier utilizes source degeneration of 200 Ω, the ENOB is improved by 0.25-bit using the SNR calculation. The actual improvement considering other parameters in the MDAC is 0.15-bit, which is analyzed in the following section. If the amplifier does not use the source degeneration, the input signal swing range is reduced and it might become a problem due to the mismatch voltage of the comparator. To compensate reduced signal swing range, the amplifier's gain has to

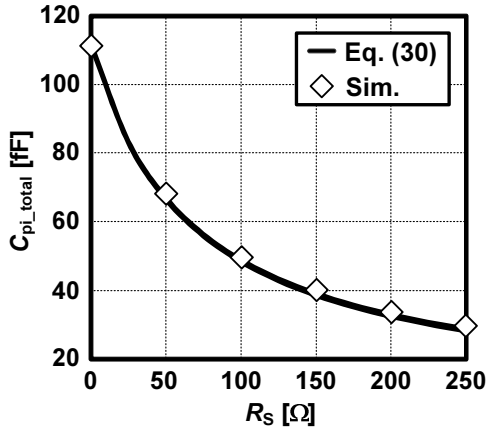



**Fig. 10** Characteristic of $C_{pi\_total}$ vs. $R_S$.

be increased. However, increasing gain degrades the settling characteristic of the amplifier. Therefore, the effort on reducing the input parasitic capacitance is important.

## 4. MDAC Stage

### 4.1 MDAC Noise Analysis

Some characteristics of the amplifier, such as the noise and the gain have to be analyzed with the MDAC stage's parameter. Several works have been published for the analysis of the MDAC stage in a pipeline ADC. [23-24] analyze the MDAC stage for the noise, the speed, and the power consumption. [25] proposes a performance model and an analysis of the MDAC for the noise and the speed characteristics. However, previous works are only applicable to the conventional pipeline topology. Therefore, an adequate MDAC model and analysis are necessary for the interpolated pipeline ADC.

Fig. 11 shows a small signal model of the MDAC stage. In Fig. 11, $R_{swi}$ is the on-resistance of the reference selection switch, $C_S$ is the sampling capacitance, $C_{pi}$ is the input parasitic capacitance of the amplifier, $C_{po}$ is the output parasitic capacitance of the amplifier, $R_{swo}$ is the on-resistance of sample and hold switch in the following stage, and $C_L$ is the load capacitance (sampling capacitance of the following stage). $g_{m\_eff}$ is the effective $g_m$ of source degeneration amplifier and $i_{nt}$ is the total noise current of the amplifier as shown in Fig. 8. The input referred noise power is represented in (31),

$$\boldsymbol{V}_{ni}^2 = \frac{\boldsymbol{kT}}{(\boldsymbol{C}_L + \boldsymbol{C}_{po})} \frac{1}{\boldsymbol{G}_{pi}^2 \boldsymbol{G}_0} \left( \frac{1}{\boldsymbol{G}_0} + \boldsymbol{G}_{pi}^2 \boldsymbol{g}_{m\_eff} \boldsymbol{R}_{swi} + \gamma \right) \quad (31)$$

where $k$ is the Boltzmann constant, $T$ is the ambient temperature, $G_0$ is the gain of the amplifier, $G_{pi}$ is the gain of the input signal path, and $\gamma$ is a transistor noise coefficient. In (31), $R_{swo}$ (and $v_{nso}$) in Fig. 11 are omitted because $R_{swo}$ is much smaller than $R_D$. The noise from the following stage is not included. $G_{pi}$ can be defined as

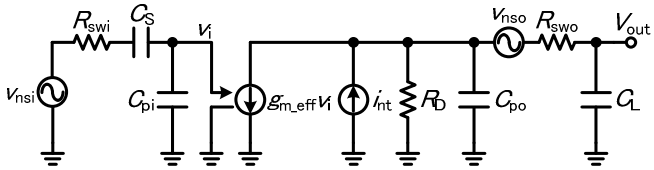



**Fig. 11** Small signal model of MDAC stage.

Table. 1 Parameters' value for noise calculation

| $V_{REF}$ [mV] | $C_S$ [fF] | $C_{po}$ [fF] | $G_{pi}$ | $G_0$ | $g_{m\_eff}R_{swi}$ | $\gamma$ |
|---|---|---|---|---|---|---|
| 600 | 320 | 57 | 0.76 | 3 | 1 | 1 |

below.

$$\boldsymbol{G}_{pi} = \frac{1}{1 + \frac{\boldsymbol{C}_{pi}}{\boldsymbol{C}_S}}. \quad (32)$$

Equation (32) shows that $C_{pi}$ degrades signal swing range and worsens the ADC's SNR performance. Therefore, the input transistor size of the amplifier has to be determined with $C_{pi}$ consideration. $g_{m\_eff}R_{swi}$ is assigned as 1. The other parameters' values are described in Table 1. On-resistance and parasitic capacitance are estimated from [8]. The ENOB of the ADC can be written as (33).

$$\mathrm{ENOB} = \boldsymbol{N} - \frac{1}{2}\log_2 \left\{ \frac{12}{\boldsymbol{V}_q^{\,2}} \frac{\boldsymbol{kT}}{(\boldsymbol{C}_L + \boldsymbol{C}_{po})} \frac{1}{\boldsymbol{G}_{pi}^2 \boldsymbol{G}_0} \times \left( \frac{1}{\boldsymbol{G}_0} + \boldsymbol{G}_{pi}^2 \boldsymbol{g}_{m\_eff} \boldsymbol{R}_{swi} + \gamma \right) + 1 \right\}. \quad (33)$$

More information for (31) and (33) are written in Appendix 1.

Fig. 12 shows the calculation and the simulation results of ENOB vs. load capacitance. The same ADC is utilized for the simulation in [8]. It is recognized that to achieve 0.2-bit of ENOB degradation, about 100 fF of the load capacitance is required. Equation (33) shows that in order to suppress the noise of the circuit, increasing $G_0$, $G_{pi}$, and $C_L$ are effective. In (33), $G_0$ is $R_D/R_S$ in the source degeneration amplifier topology. The gain is determined by the comparator's mismatch voltage. If the gain is increased by $R_D$, the bandwidth is degraded. $G_{pi}$ is increased by large $C_S$; however, large $C_S$ increases input driver difficulty. The load capacitance $C_L$ affects both the noise performance and the bandwidth; therefore it has to be determined considering both of the effects. As described above, relationship between the parameters and the ADC's performance are complicated. Detailed design flow to determine the ADC's parameters are shown in Section 6.

### 4.2 ADC Performance with Gain Variation

In this section, the variation of the sampling speed ($F_S$) and the ENOB with changing amplifier's current ($I_D$) will be analyzed. The values of the parameters for the calculation and the simulation are the same values given

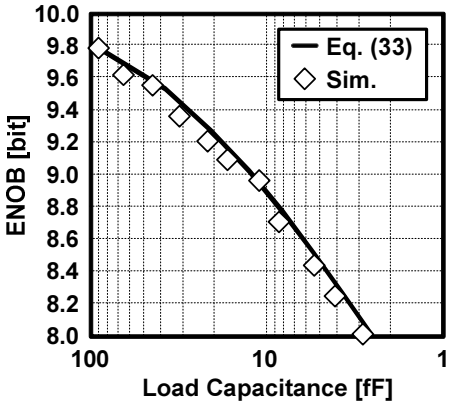



**Fig. 12** ENOB vs. load capacitance of amplifier.

in the Table 1. The load capacitance of the amplifier is set as 100 fF to achieve a 0.2-bit ENOB degradation, which is determined by Fig. 12. Comparator's latch time is set as 200 ps, which is estimated from the circuit in [8]. $F_S$ is calculated by the settling time and comparator's latch time. The settling time is calculated within 1/4 LSB error, which is considered as the worst case. ΔENOB is calculated based on (33) when the ADC's resolution is 10-bit. From Fig. 13 to Fig. 14, the solid lines are calculation results and the symbols are simulation results.

First, the default condition performance is examined to help the understanding for further analysis. The calculation and the simulation results are shown in Fig. 13. $F_S$ becomes faster with increasing $I_D$. However, the growth of $F_S$ slows down significantly after 5-6 mA in Fig. 13 because of the increase of the parasitic capacitance. Due to the same reason, the input signal swing range is also reduced and it causes performance degradation of the ADC as represented in (31) and (32). In Fig. 13, the ENOB is degraded by 0.3-bit when $I_D$ is 8 mA (simulation) and the degradation grows to 1-bit when $I_D$ reaches 40 mA. Using this analysis, below 6 mA current shows reasonable performance with 1-2 GS/s and 0.2-0.3 ENOB degradation.

In Fig. 13, the simulation and the calculation shows good matching in speed. However, there is a 0.1-bit difference in ENOB results from 2 mA to 10 mA. This may be caused by the influence of noise characteristics due to other parasitic components. Less than 1 mA current, the noise of the simulation results increases due to 1/f noise, which is not considered in the calculation.

Fig. 14 shows the ADC's performances by changing the amplifier's gain. The gain is controlled by the output resistance, $R_D$. In Fig. 14, increasing the gain of the amplifier improves the ADC's SNR. However, increased $R_D$ causes narrow bandwidth of the amplifier and it degrades $F_S$. The results with different gains can be adjusted to the default results (shown in Fig. 13) by changing the load capacitance, $C_L$. For example, $F_S$ and ΔENOB are almost same when $G_0$=3, $C_L$=100 fF and $G_0$=4, $C_L$=70 fF. Decreased $C_L$ causes increasing noise

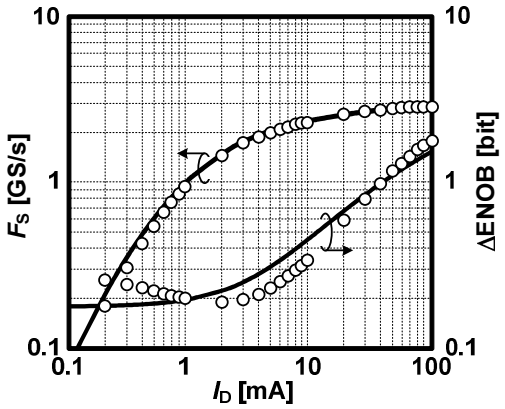



**Fig. 13** $F_S$, ΔENOB vs. $I_D$.

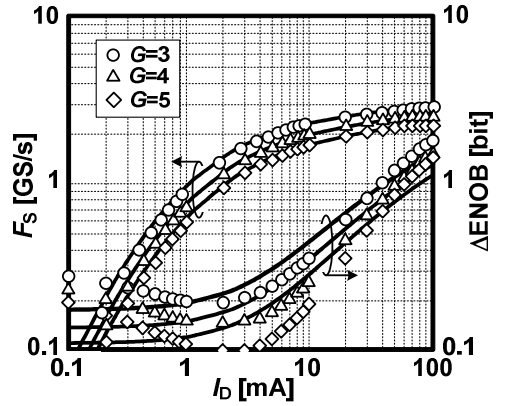



**Fig. 14** $F_S$, ΔENOB vs. $I_D$ with gain variation.

and mismatch; however, increased gain cancels those degradations. Moreover, decreased $C_L$ brings advantages of bandwidth and area. Therefore, within the allowance of the linearity of the amplifier, it is better to use higher gain amplifier with smaller load capacitance.

## 5. Pipeline Stage Resolution

The interpolated pipeline ADC can be designed with any resolution in its pipeline stage. In the interpolated pipeline topology, one of the most important criteria to determine the resolution of the stage is the power consumption. The pipeline stage consists of 3 parts, which are amplifier, sub-ADC, and interpolator. In these parts, the interpolators do not consume much power because they charge and discharge its input signal dynamically. Therefore, the power consumption is determined by the amplifier and the sub-ADC. For example, two amplifiers in 4-bit stage occupy 67 % of total analog power consumption.

The power consumption and circuit size in the sub-ADC increases with $2^{N1st}$, where $N_{1st}$ is the resolution of the 1st stage. Although the power consumption of each comparator is small, it increases exponentially with the resolution increase. Therefore, it is desirable to have a low resolution for the sub-ADC. On the other hand, the power consumption of the amplifier is a function of $g_m$. As explained in Section 3.2, there is a trade-off between

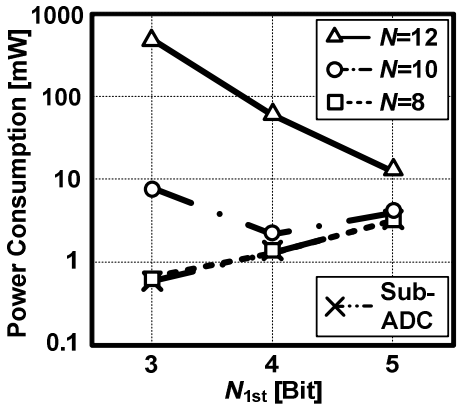



**Fig. 15** Power consumption vs. resolution in stage.

the linearity requirement and the stage resolution. Assume that the ADC's resolution is 10-bit and $V_{FS}$ is 0.6 V. For a 4-bit resolution of the 1st stage, to achieve the ENOB degradation less than 0.2-bit, about 3.7 of $a_3/a_1$ is required. However, $a_3/a_1$ requirement becomes more severe to less than 0.45 for a 3-bit stage resolution because the output swing range of the amplifier is inversely proportional to the stage's resolution. And amplifier's linearity becomes worse with increasing signal swing. Therefore, increasing stage resolution makes it possible to use smaller $g_m$ for the amplifiers to achieve the same ADC performance. Furthermore, it contributes to the small power consumption. The $a_3/a_1$ requirements in this paragraph are based on (15) and (22).

As described above, the power consumption of the sub-ADC and the amplifiers have an inverse proportional relationship. The calculation results of the power consumption vs. stage's resolution are shown in Fig. 15. Parameters for the calculation are estimated from the circuit in [8] with 320 MHz sampling speed. Three ADC resolution examples are shown in Fig. 15, such as 8, 10, and 12-bit for 3 to 5-bit stage resolutions. The optimized stage resolutions are different in each case. For example, for an 8-bit ADC, the linearity requirement is not severe; therefore, the power consumption is almost determined by the sub-ADC. In this case, source degeneration might not necessary. However, for 10-bit ADC, the linearity requirement becomes severe. Up to 4-bit stage resolution in 10-bit ADC, large $g_m$ for the linearity is the main reason of the large power consumption. Therefore, the power consumption is decreased with stage resolution increasing. However, when the stage resolution becomes 5-bit, the linearity requirement becomes much more relaxed and the power consumption of the amplifier is also reduced. Even though required $g_m$ becomes smaller, total power consumption is increased because of the increased number of the comparator. For a 12-bit ADC, the linearity requirement becomes more severe. This causes large power consumption of the amplifiers. In that case, the linearity requirement can be relaxed by using a 5-bit stage resolution. For 12-bit ADC, it may be better to use higher gain op-amp with feedback loop to reduce power consumption. 1 and 2-bit stage resolution are not considered in this analysis because it is impossible to achieve 1-bit redundancy with below 2-bit structure by the interpolation.

## 6. Design Flow

Similar to the conventional pipeline ADC, the amplifier determines the performance of the interpolated pipeline ADC. However, the important point is not the gain but the linearity and the noise due to its low-gain characteristic and open-loop usage. To achieve the target performance, linearity enhancement technique is essential such as source degeneration.

To design an interpolated pipeline ADC, a reasonable design flow to determine the component parameters is shown in Fig. 16. When the ADC specification is given, designers have to examine the validity of the interpolated pipeline topology for the given specification. The validity can be checked by Fig. 13. If the interpolated pipeline is determined as a suitable topology, the resolution of the stage can be optimized by Fig. 15.

The ADC's performance can be represented by the operating speed and the resolution. After the stage resolution is determined, other parameters have to be assigned to satisfy the target speed and resolution. The resolution is affected by the linearity and the noise characteristics. For the linearity, $g_mR_s$ is calculated by $a_3/a_1$ requirement for the given ADC specification, using (15) and (22). The noise requirement is achieved by selecting a proper value for $C_L$, which is shown in Fig. 12. On the other hand, $C_L$ affects to the bandwidth. Also, $R_D$ is a parameter for the bandwidth. Because $C_L$ is already defined, $R_D$ can be calculated for the bandwidth requirement. After that, $R_S$ is determined by the gain, which is determined by the comparator's mismatch voltage. Through above design flow, designers can estimate the required values for the parameters to achieve target specification.

## 7. Conclusion

In this paper, the design of the interpolated pipeline ADC using low-gain open-loop amplifiers has been introduced. The interpolated pipeline topology allows high resolution ADC to be realized with low-gain amplifiers by using the interpolation technique. To realize the ADC without any MDAC calibration, parameters of the amplifiers and the MDAC have to be determined based on proper analysis, especially for the linearity, the noise, and the settling time. In this paper, the linearity requirement and the noise characteristic of the amplifier are analyzed. Through the given analysis, the required parameters of the amplifier become clear, such as $g_mR_S$. Also, the noise analysis of MDAC suggests the value of $C_L$ with considering the ENOB degradation. The performance

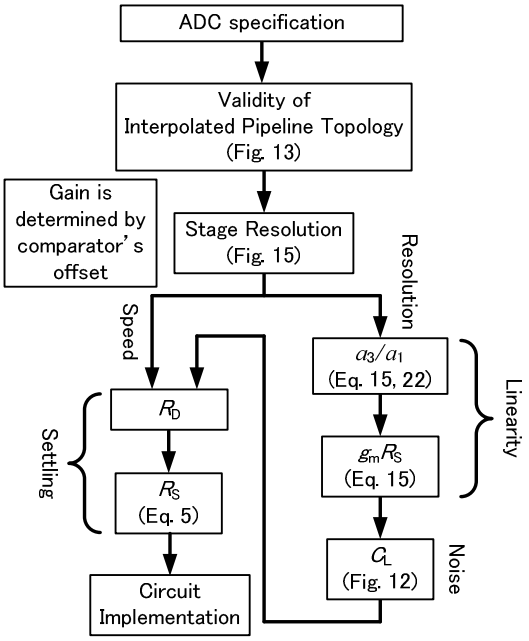



**Fig. 16** Design flow.

limitation of the interpolated pipeline ADC is shown by $F_S$ and ΔENOB vs. $I_D$ with the amplifier's gain variation. Finally, the stage resolution optimization is discussed based on the power consumption. Through the above analysis, $g_m$, $R_S$, $R_D$, and $C_L$ are determined for the target specification. The analysis in this paper is organized in Fig. 16 as a design flow chart. The analysis shows that the interpolated pipeline ADC is suitable for the recent scaled technology and has a strong potential for future development.

## Acknowledgments

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## Appendix. I

From Fig. 11, a formula can be derived for the output noise power ($V_{no}^2$) with consideration of the frequency as below.

$$V_{no}^2 \approx 4kT\left\{\left(\gamma g_{m\_eff} + \frac{1}{R_D}\right)R_D^2 + R_{swi}\left(G_{pi} g_{m\_eff} R_D\right)^2\right\}\int_0^\infty \frac{1}{1+\left(\frac{f}{f_L}\right)^2} df. \quad (34)$$

Parameters in (34) are the same as explained in Section 4.1. Also, the effect of $R_{swo}$ in Fig. 11 is omitted. In (34), $f$ means frequency and $f_L$ means the cut-off frequency. Equation (34) can be arranged as

$$V_{no}^2 = 4kT\left\{\gamma g_{m\_eff} R_D^2 + R_D + R_{swi}\left(G_{pi} g_{m\_eff} R_D\right)^2\right\}\frac{\pi}{2} f_L. \quad (35)$$

Equation (35) can be reorganized by substituting $f_L$ to the output resistance and capacitance.

$$V_{no}^2 = kT\left\{\gamma g_{m\_eff} R_D^2 + R_D + R_{swi}\left(G_{pi} g_{m\_eff} R_D\right)^2\right\}\frac{1}{R_D\left(C_L + C_{po}\right)}. \quad (36)$$

The output parasitic capacitance is considered for the accurate calculation. Equation (36) is rewritten as

$$V_{no}^2 = \frac{kT}{\left(C_L + C_{po}\right)}\left\{1 + R_{swi}\left(G_{pi} g_{m\_eff}\right)^2 R_D + \gamma g_{m\_eff} R_D\right\} \quad (37)$$

To obtain the input referred noise power, the output noise power has to be divided by gain.

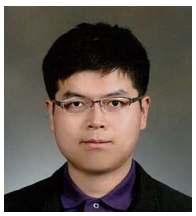
$$V_{ni}^2 = \frac{kT}{\left(G_{pi} G_0\right)^2\left(C_L + C_{po}\right)}\left\{1 + R_{swi}\left(G_{pi} g_{m\_eff}\right)^2 R_D + \gamma g_{m\_eff} R_D\right\} \quad (38)$$

As explained in Section 4.1, the signal path gain $G_{pi}$ is also considered to figure out the effect by the input parasitic capacitance of the amplifier. Lastly, equation (38) can be reorganized to (31) by substituting $G_0$ to $g_{m\_eff}R_D$.

The input referred noise power with consideration of the ENOB degradation is expressed as below [26].

$$V_{ni}^2 \approx \left(2^{2\times\Delta ENOB} - 1\right)\frac{V_q^2}{12}. \quad (39)$$

By substitute $V_{ni}^2$ in (39) to $V_{ni}^2$ in (31), the ENOB degradation can be expressed as (33).



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